

Manchester encoder–decoder for optical data communication links

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A new encoder–decoder (CODEC) design of a Manchester coding scheme suitable for optical data communication links is presented. The design is simple and uses off-the-shelf digital electronic components and subsystems. The CODEC can be used for high data rate transmissions, typical of optical fiber systems and local area networks. The decoder is insensitive to variations in the clock rates within the range of $\pm 33\%$, whereas the encoder, which is a simple XOR logic gate, is not affected by clock variations. During high-frequency operation (e.g., at 100 MHz), the CODEC can be operated at a wide range of frequencies (from 66.6 to 133.3 MHz) without modification to the CODEC circuitry. Furthermore, the CODEC can be made to operate at any data rate by a simple change of a single capacitor or a single resistor in the decoder circuit. The CODEC was built in the laboratory by using transistor-transistor logic integrated circuits. It was experimentally found that with this decoder the transmitted data, as well as the clock, can be recovered from the Manchester coded signal without being affected by clock variations within the designed range.

I. Introduction

As an application of the Manchester coding scheme, consider a typical optical fiber communication system, whose block diagram is shown in Fig. 1.¹ The main function of the optical source is to convert the electrical signal into an optical one, with suitable power for transmission over the fiber. At the receiver, the optical detector reconverts the optical energy into an electrical one. The design of such subsystems is widely published.¹ Because of the high bandwidth of the optical fiber system, it is important to use it in a serial transmission mode. This can be achieved by encoding the data to have the desired characteristics. Although several digital coding schemes are available, the Manchester code (Fig. 2) has the advantage of being a self-clocking code, as there is always a transition at the mid-bit interval. A unipolar code is preferred for optical fibers, and, furthermore, the absence of an expected transition can be used for error detection.²

Several encoder–decoder (CODEC) circuit implementations are available.^{3–6} These circuits, however, seem to be limited in frequency,³ use more components,^{4,5} or use phase-locked loops⁶; in all these

circumstances a large amount of lock-in time is required for high data rates. In this paper a new design is presented that operates at any data rate, uses a smaller number of components, and operates at a wide range of frequencies without the need to modify the CODEC circuitry.

II. System Design and Operation

The Manchester encoder is simple and can be implemented as a single exclusive OR gate by using a clock whose frequency is equal to the data rate as shown in Fig. 3. The clock and data must be synchronized to avoid glitches in the output. The encoder operation is illustrated by the first three lines, which are transmitted data (TD), transmitted clock (TC), and encoded data (ED) (see Fig. 5). It is clear that the encoder will work with any set of data at any rate, and therefore we do not discuss the decoder further here.

The main function of the decoder is to reproduce the system clock as well as the transmitted data from the received Manchester encoded signal. The circuit uses one shot integrated circuits (IC's) (e.g., 74LS121), as shown in Fig. 4. The decoder operation is explained in Fig. 5. A test pattern (TD) of 0100110 is fed to the encoder (XOR) input and its output (ED) is connected to the decoder input. The received data (point 6 in Fig. 4) and the received clock (point 5 in Fig. 4) are shown in Fig. 5 together with intermediate waveforms at each stage of the decoder. It is clear that the decoder will work with any data stream and will not

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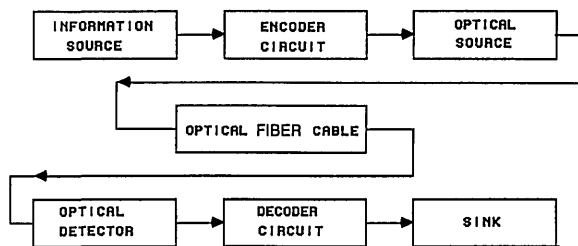


Fig. 1. Simplified optical fiber communication system.

D A T A	0		1	
C L O C K	0	1	0	1
O U T P U T	0	1	1	0

Fig. 2. Manchester encoding scheme.

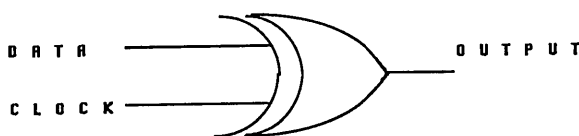


Fig. 3. Manchester encoder.

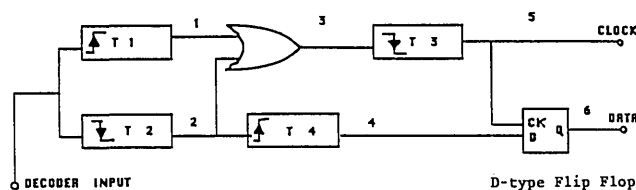


Fig. 4. Manchester decoder.

be affected by consecutive ones or zeros, as illustrated by this example.

In Fig. 4, the two one shots, T1 and T2, are used as transition detectors: T1 for positive transitions and T2 for negative ones. The system clock information is embedded in these transitions, and, to extract this clock, an OR gate and T3 are used as shown in Fig. 4. It is clear that there are two pulses per one clock period at the output of the OR gate if the input signal to the decoder has two or more successive ones or consecutive zeros. For correct clocking of the decoder, this extra pulse must be eliminated. This can be achieved by choosing a T3 output pulse (τ_3) value such that it marks this extra pulse, i.e., a minimum of $0.5T$ as shown in Fig. 6A, where T is the system clock period. The maximum value of τ_3 should not exceed T ; otherwise the pulse identifying the next digit will be lost (Fig. 6B). Therefore, τ_3 must be in the range

$$0.5T < \tau_3 < T. \quad (1)$$

These values represent the upper and lower limits of τ_3 for the designed frequency of operation f_o , where $f_o = (1/T)$. The middle value of $\tau_3 = 0.75T$ is chosen for safe operation (Fig. 6A). $\tau_3 = 0.75T$ having been fixed, the decoder will work properly if the clock

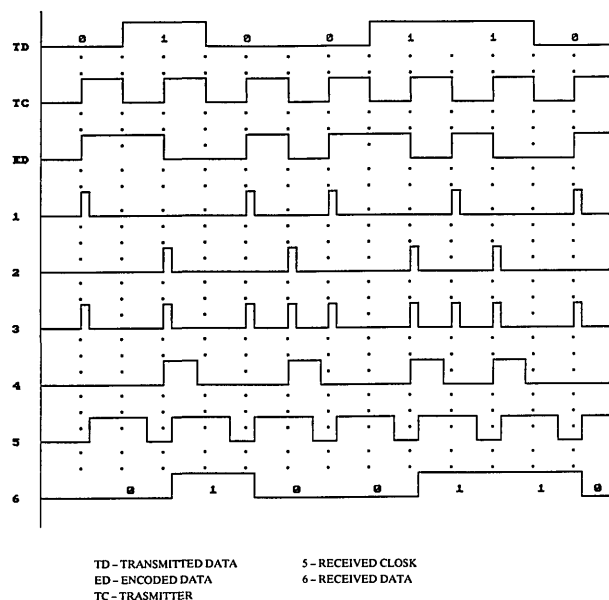


Fig. 5. Timing diagram of the Manchester decoder.

period is not greater than $1.5T$ (T_{high}) and not less than $0.75T$ (T_{low}) (Fig. 6B). These values correspond to the frequency range

$$(2/3)f_o < f < (4/3)f_o, \quad (2)$$

i.e., the decoder that is designed for a system frequency of f_o will still operate correctly with a system clock variation of $\pm 33\%$. Obviously, this tolerance is governed by the performance of the available components, especially the rise and fall times of the digital IC's. Rise and fall times may be minimized by using

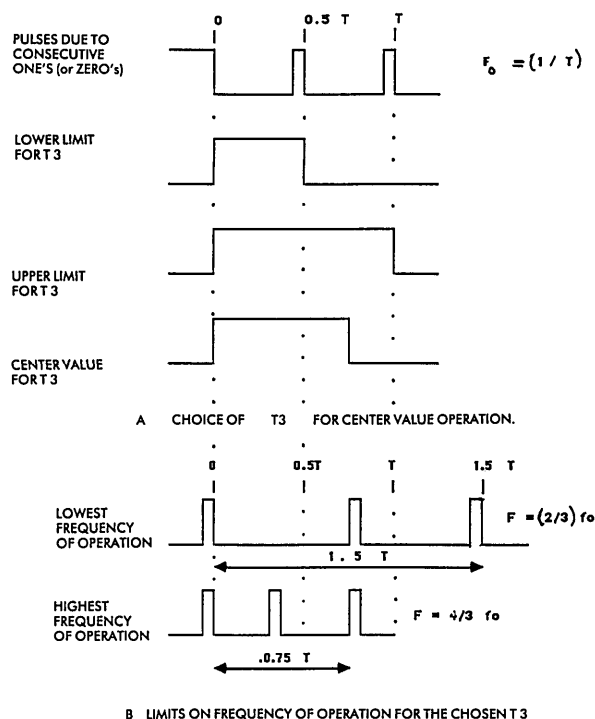


Fig. 6. Range of frequency of operation for the decoder circuit.

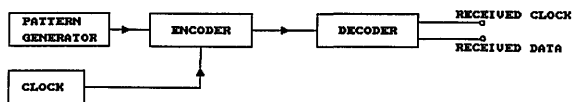


Fig. 7. CODEC test circuitry.

fast switching devices such as the emitter coupled logic series. This range could be significant if the CODEC center frequency were designed to be high (e.g., 100 MHz). Then it would work in the frequency range 66.7–133.3 MHz, i.e., a bandwidth of 66.6 MHz. Furthermore, the system may be modified to operate at different speeds by changing τ_3 , i.e., by changing one resistor or a single capacitor of the T3 one shot of the decoder.

Careful inspection of Fig. 5 indicates that the output data are delayed by

$$\text{delay} = 0.5T + \tau_2. \quad (3)$$

This delay can be ignored, especially when working with high data rates. Additionally, assuming a propagation delay of T_p per stage, the received data will be delayed by $4T_p$. If the clock period is chosen such that it is larger than the total propagation delay, clock slips will not occur.

The output pulse durations of T1 and T2 one shots are chosen such that

$$\tau_1 \ll T, \quad (4a)$$

$$\tau_2 \ll T; \quad (4b)$$

then τ_4 is chosen such that it is greater than τ_1 and less than $0.5T$. However, because the clock period is permitted to shrink to $0.75T$, τ_4 must be selected to satisfy the following:

$$\tau_1 < \tau_4 < 0.375T. \quad (5)$$

The duty cycle of the clock is initially fixed at 75%, but this duty cycle will change with the clock variations. The limits for the duty cycle are 50% (when the clock period expands to $1.5T$) and 100% (when the clock period shrinks to $0.75T$). This issue is not critical, as our main interest is to recover the data and the clock period.

III. CODEC Implementation and Testing

The CODEC was built in the laboratory by using standard transistor-transistor logic IC's. The test

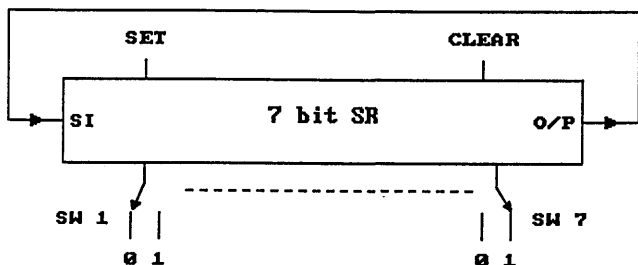


Fig. 8. Pattern generator.

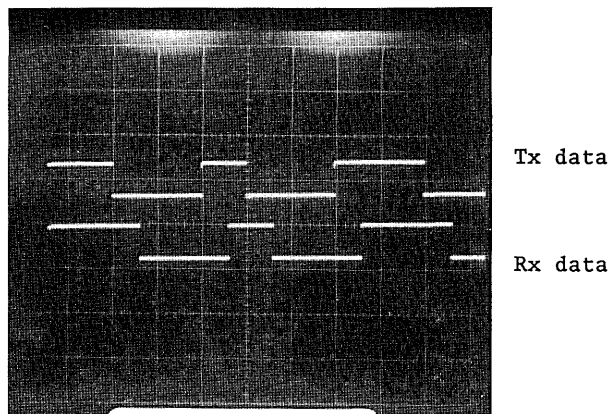


Fig. 9. Transmitted (Tx) and received (Rx) data.

circuitry used is shown in Fig. 7. The system clock was taken from a transistor-transistor logic compatible clock generator and was set at 10 kHz. In order to observe the pattern on the scope, it was made repetitive by using a 7-bit parallel-in serial-out feedback shift register, as shown in Fig. 8. The feedback shift register is first loaded with the required pattern and then cyclically shifted to the right. The test data pattern discussed in Section II was generated and fed to the encoder input. The encoder output is connected to the decoder input.

Practical CODEC waveforms are the same as those shown in Fig. 5 and therefore are not included here. Figure 9 contrasts the transmitted and the received data and illustrates the delay in the received data. Figure 10 depicts the transmitted and the received clock data and demonstrates the difference in duty cycle between them.

The one-shot output pulse durations were designed to have the following values:

$$T = 100 \mu\text{s},$$

$$\tau_1 = 10 \mu\text{s},$$

$$\tau_2 = 10 \mu\text{s},$$

$$\tau_3 = 75 \mu\text{s},$$

$$\tau_4 = 30 \mu\text{s}.$$

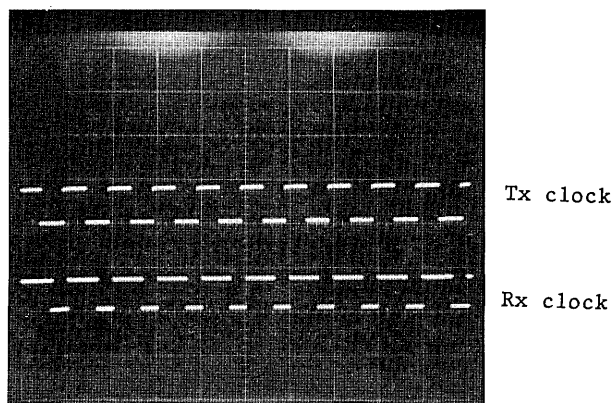


Fig. 10. Transmitted (Tx) and received (Rx) clock.

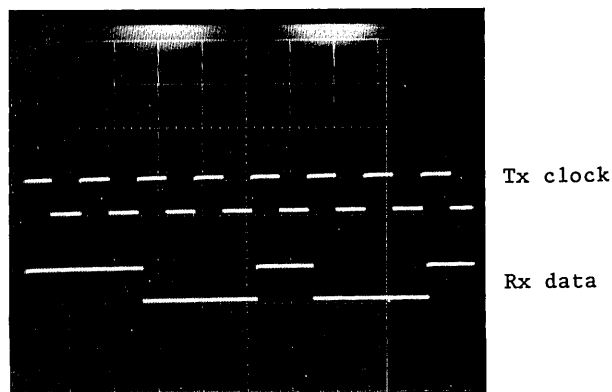


Fig. 11. Maximum operating frequency.

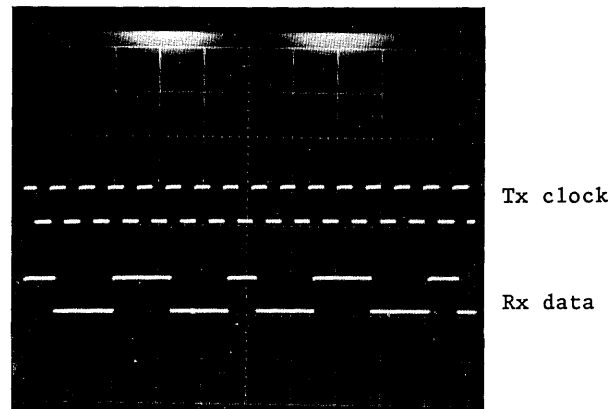


Fig. 12. Minimum operating frequency.

The transmitter (encoder) clock was varied between 15.226 and 7.656 kHz without loss of data, and the results obtained are shown in Figs. 11 and 12. In both figures, the top traces represent the transmitted clock rate, whereas the bottom traces display the received data. For the chosen operating frequency of 10 kHz, the upper and the lower values are expected to be 13.333 and 6.667 kHz, respectively. This discrepancy between the designed and the practical values results because τ_3 was not exactly equal to 75 μ s but was equal to 65.5 μ s (i.e., $0.655T$). If this 65.5 μ s corresponds to the center operating frequency, then the upper and the lower frequencies of operation will be 15.263 and 7.626 kHz, respectively. This agrees with the practical results, with a small difference that is due mainly to inaccuracies in clock frequency adjustment.

The whole CODEC can be implemented on a single medium scale integration chip. In this chip, τ_1 , τ_2 , and τ_4 are fixed internally to operate at the highest possible operating frequency of the technology used. At any lower frequency τ_1 , τ_2 , and τ_4 will satisfy inequalities (4) and (5), thus reducing to two the number of external components that the user needs to connect: resistor and a capacitor determining τ_3 .

IV. Conclusions

A simple optical data communication link using the Manchester coding scheme has been presented. At the heart of this link is a new Manchester CODEC design that uses only digital IC's. The CODEC was built and tested in the laboratory, and it was found

that the experimental results agree with the theory. The encoder is made of a single XOR logic gate that can operate, depending on the limitation of the IC technology used, at any desired frequency. The decoder is easy to implement and uses four one shots, one OR gate, and one D-type flip-flop. It can retrieve both the transmitted data and clock. It operates at any data rate and is insensitive to system clock variations within $\pm 33\%$ tolerance. This range is significant when the designed operating frequency is high (e.g., at 100 MHz, this corresponds to a 66.6-MHz range). The CODEC can be operated at any other data rate by simply changing a single capacitor or a resistor governing the output pulse duration of a single one shot (T_3) in the decoder circuit. The whole CODEC can be implemented on a single medium scale integration chip with only two external components.

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